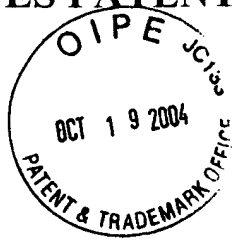


# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## In re Application of :

Zhaohui Shen  
Daniel Watkins



## Serial No. :

09/684,868

## Group Art Unit :

2825

## Filed :

October 06, 2000

## Examiner :

Dinh, Paul

## For :

Diagnostic Architecture Using  
FPGA Core in System on a Chip  
Design

## Atty Docket :

1496.00039 / 00-255

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Mark Salvatore

October 19, 2004

Date

Signature

## SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

## Official Draftsman

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation  
1621 Barber Lane, MS D-106  
Milipitas, CA 95035  
408-433-7475

Respectfully submitted,

Henry Groth

Reg. No. 39,696

Date: 10/15/2004